

THE UNIVERSITY OF ADELAIDE

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING ADELAIDE, SOUTH AUSTRALIA 5005.

B.E. in Electrical and Electronic Engineering B.E. in Computer Systems Engineering B.E. in Information Technology and Telecommunications

ELEC ENG 4039 A/B HONOURS PROJECT FINAL REPORT

Each student at Level IV of the course in Electrical and Electronic Engineering, Computer Systems Engineering and Information Technology and Telecommunications is required to complete this course. The course involves approximately 240 hours of project work over the whole academic year. Students are assessed on their performance in the project, a written proposal, this written report, a technical paper, and two seminar presentations.

Date submitted:

Supervisor: Matthew Sorell

Signature of Supervisor:



Assessment Cover Sheet

Student Name	Timothy Robert Ansell
Student ID	1091790
Assessment Title	Develop a multiple FXS to PC bridge (MS2/1)
	Final Report
Course/Program	B.E. in Information Technology and Telecommunications
Lecturer/Tutor	Matthew Sorell
Date Submitted	
OFFICE USE ONLY	
Date Received	

KEEP A COPY

Please be sure to make a copy of your work. If you have submitted assessment work electronically make sure you have a backup copy.

PLAGIARISM AND COLLUSION

Plagiarism: the use of another person's ideas, designs, words or works without appropriate acknowledgement.

Collusion: assistance in the production of an assessment submission without the express requirement, or consent or knowledge of the assessor.

CONSEQUENCES OF PLAGIARISM AND COLLUSION

The penalties associated with plagiarism and collusion are designed to impose sanctions on offenders that reflect the seriousness of the University's commitment to academic integrity. Penalties may include: the requirement to revise and resubmit assessment work, a result of zero for the assessment work; failing the course, expulsion and/or a financial penalty.

I declare that all material in this assessment is my own work except where there is clear acknowledgement or reference to the work of others. I have read the University Statement and Definition of Plagiarism and Related Forms of Cheating (<u>http://www.adelaide.edu.au/policies/?230</u>).

I give permission for my assessment work to be submitted for electronic checking of plagiarism.

Signed..... Date

PLEASE SIGN HERE

1 - Abstract

This document outlines the progress and results for the Final Year Honours Engineering project "Develop a multiple FXS (Foreign Exchange Station¹) to PC bridge (MS2/1)".

The project set out to produce a low cost device to interface all telephones in a single premises to a PC. The target price point was for the device to be sold to the consumer for under \$US150, significantly undercutting the current market. A "proof of concept" prototype board has been built and demonstrates the real possibility of achieving the goal of the final low cost solution.

The progress of the project is examined and reflections on the project management, including risk mitigation, resolution and impact are discussed.

During the development of this project a number of modifications and improvements needed to be made to the original proposal. The rational for these modifications and how they effected the production cost is explained. Information on how to take the device from the prototype stage into the commercial production and comparison between a final device and potential competitors, both on price and features, is also a another component of this document.

From the knowledge gained in developing the prototype, discussion of potential further developments, including feature enhancements and further cost reductions is presented. There are also proposals for other related projects and other potential profitable endeavours.

The document also has a full Technical and Programming Datasheet for the prototype board in the Appendix. The datasheet includes the performance characteristics of the current device, programming specifications and documentation of the example test code.

¹ A FXS interface is a telephone interface which provides battery power, sends dial tone, and generates ringing voltage allowing connection to a standard telephone.

Table of Contents

1 - <u>Abstract</u>	3
2 - <u>Acknowledgements</u>	7
3 - <u>Aim</u>	8
4 - Project Summary	8
5 - <u>Related Projects</u>	10
6 - <u>Background</u>	11
6.1 - <u>Development Justification</u>	11
6.2 - Current Competition	12
Linksys SPA2002-ER	13
BiPAC 6404V	13
 Digium TDM880B	14
7 - <u>Project Overview</u>	15
8 -Project Changes	16
Conversion to CODECs	16
Removal of Port Extender	17
 <u>Block Diagram</u>	18
9 - Project Progress	20
<u>USB PIC – Breadboard Prototype</u>	20
<u>USB PIC – Veroboard Prototype 1</u>	20
<u>USB PIC – Veroboard Prototype 2</u>	22
<u>USB PIC – Milled Prototype</u>	22
SLIC Chip – Breadboard Prototype	23
SLIC Chip – PCB Prototype	24
Port Extender Chip – Breadboard Prototype	25
DAC Chip – Breadboard Prototype	26
CODEC – Breadboard Prototype.	26
Prototype Board – Milled Prototype 1	27
Prototype Board – Milled Prototype 2	28
Prototype Board – Commercial PCB Prototype	29
10 - <u>Risk Management</u>	32
10.1 - <u>Computer Related Risks</u>	32
10.2 - Design Based Risks	32

Filter Expense	32
CODEC Behaviour	33
Power Supply	33
Software Problems	
10.3 - <u>Supply Chain Risks</u>	34
PCB Manufacture	34
11 - <u>Project Spending</u>	35
12 - <u>Production Budget</u>	
13 - <u>Commercial Device</u>	40
13.1 - <u>Size Reduction</u>	40
13.2 - <u>Packaging</u>	40
13.3 - Using Different CODEC	41
14 - <u>Further Developments</u>	43
Cost Reduction Developments	43
Combining of Shift Register data lines	43
High IO USB PIC Version	43
Replace PIC with DSP processor	43
Higher Density Chip Version and Small SMD components	44
Feature Enhancement Developments	44
Ethernet PIC Version	44
Asterisk PBX Interface	45
Line Line Support	45
Direct Connection	45
14.1 - Internal Telephone Interface Cards	48
VoIP Handsets	48
Gateways	

Appendix I - Technical Document – MITHIS CFXS Datasheet	46
Appendix II - Further Background Information	48
Appendix III - List of Acronyms	50

Table of Illustrations

Illustration 1: Original System Block Diagram	
Illustration 2: Final System Block Diagram	19
Illustration 3: USB PIC – Breadboard Prototype Picture	20
Illustration 4: USB PIC – Veroboard Prototype 1 Picture	21
Illustration 5: USB PIC – Veroboard Prototype 2 Picture	22
Illustration 6: USB PIC – Milled Prototype (Large Version) Picture	23
Illustration 7: USB PIC – Milled Prototype (Small Version) Picture	23
Illustration 8: SLIC Chip – Breadboard Prototype Picture	24
Illustration 9: SLIC Chip – Milled Prototype Picture	25
Illustration 10: SLIC Chip – TIM Module Picture	25
Illustration 11: PE IC – Breadboard Prototype Picture	26
Illustration 12: CODEC IC – Breadboard Prototype Picture	27
Illustration 13: System Board – Milled Prototype 1 Picture	27
Illustration 14: Chip Removal Damage	
Illustration 15: System Board – Milled Prototype 2 Picture	29
Illustration 16: System Board – Commercial PCB Prototype Picture	29
Illustration 17: Populated Commercial PCB Board	
Illustration 18: Prototype Boards Compared	
Illustration 19: Possible Packaging Examples	40
Illustration 20: Intersil HC55185 - High Density QFN compared to PLCC	44

Table of Tables

Table 1: Project Spending	
Table 2: Prototype Board Production Costs	
Table 3: TIM Module Production Costs	

2 - Acknowledgements

I would like to thank the following people for their support in project development:

Matthew Sorell	Who provided advice and support and was the supervisor for this project.
David Knight	Who helped with software debugging and general advice.
Pavel Simcik	Who provided advice about the procurement of samples and helped with PCB manufacture, component soldering and hardware debugging.
Geoff Pook and Rob Garret	Who both provided advice about and assisted with hardware development, PCB manufacture and component soldering.
Matthew Trinkle	Who assisted with loaning advanced equipment that was needed for debugging the more complicated parts.

3 - Aim

The aim of this project was to produce a **low cost** device for interfacing **all** internal telephone lines in a single premises to a computer. Achieving a low production cost was the primary consideration in the development of the device. The success of the project was demonstrated by the low production cost of the prototype board and the large number of potential cost reductions identified when producing a commercial version.

The price point the project targeted was for the device to retail in the consumer market for under \$US150². This is significantly less that the current competitors, which either provide only one or two telephone interfaces, or cost upwards of \$US700³.

The typical application for the device produced in this project is to build computer based PBXs for use in homes or small businesses. By using a computer based PBX, support for interfacing older POTS telephones to VoIP technologies, such as H323, SIP and Skype is easily achieved.

4 - Project Summary

This project was strongly based in development rather than the more common research project. The project had a primary focus on a final outcome of a commercial producible device. Solutions which would normally have been made to save development time but increase production costs had to be discarded. This more realistically mirrors the development process used in the consumer electrical products industry, where development time is amortised over millions of units.

By the end of the project, a number of prototype boards had been produced, and software which demonstrated its function had been developed. The progress this project made, demonstrated that the overall outcome, that of a device which could be sold on the consumer market for \$US 150, is a clear possibility. Only a small amount of further development is required to fully achieve this goal.

During development, a number of further development options were discovered (such as an Ethernet variant). These developments increase the retail scope of the project beyond that which the original proposal had foreseen and could dramatically increase the scope of potential markets and

² A rule of thumb says that the production cost should be around 1/3rd the final retail price, giving a production cost around \$US 50.

³ One example device is the Digium TDM880B.

therefore increase sales.

As well, during development, a number of significant tools were identified as not being available (within satisfactory cost requirements). These gaps in currently available products could also be profitably exploited with minimal development. Some examples of these include: a PIC development board which is based around Ethernet; or USB PIC devices with integrated boot loader (specifically ones which do not require Administrator access on a Windows computer).

This report covers the project development, progress and management. For full technical details see the Technical and Programming Datasheet in the Appendix.

5 - Related Projects

This project was collaborated with a number of other Final Year projects.

One of the projects that collaboration occurred with was the "Design an 8-Port Stand Alone Telephone Exchange (MS1/2)". This project required a compact and convenient way to interface telephones to their design. The project decided to use the TIM modules developed in this project to help them achieve their goals and purchased 4 modules.

Another project where collaboration occurred was the "GSM Payphone (MJS1/2)". The PIC prototype boards developed by this project have been used by the project to kick start their development.

6 - Background

Digital interfaces to telephones have been around since the late 1980s. With the advent of broadband Internet it has become easy to carry voice data over the Internet. These standards are referred to as Voice over Internet Protocol and abbreviated to VoIP. This development has dramatically reduced the cost of developing telecommunication systems and allowed numerous new features to be developed.

Many companies currently provide VoIP services, from PBX systems to PSTN termination all over the world. The VoIP industry is estimated to be worth more than \$2 billion dollars and has had a growth of over 300% in the last 5 years⁴. The device when connected to a computer based PBX system (such as Asterisk, the Open Source PBX Software system) will allow standard telephones in a business or household to communicate with almost any VoIP system in existence.

Further background information about digital telephone interfaces and VoIP technologies were outlined in the project proposal "Develop a multiple FXS to PC bridge (MS2/1) Project Proposal". A starting point for the development of the device required investigation into what devices currently exist. The requirements were then derived so that the project would perform well against the currently available devices.

6.1 - Development Justification

The limited number of lines in currently available devices do not fully exploit the potential VoIP systems can provide. Devices which do provide numerous lines are not priced at the home consumer or small business. By providing a way to interface a large number of lines, it becomes feasible to have every telephone on a separate line. This opens up a large number of possibilities which currently are not available.

Required number of Lines

The number of lines the device allowed was of considerable importance. Current devices only allow interfacing one or two lines in a premises, while this projected aimed to provide one line per room and thus outfit a whole house. To establish an estimate of the number of lines needed on the device, it is assumed that each phone handset will be on a separate line to allow individual operation of each phone simultaneously. Based on Australian Bureau of Statistics data:

⁴ Insight Research Corporation, "Worldwide Telecom Industry Growth in 2006", 2006

"The majority (57%) of separate houses had three bedrooms while a further 29% had four or more bedrooms."⁵

The average house also has additional rooms approximately equal to the number of bedrooms in each house. This means that 86% of Australian households have 6 or more rooms. It is also assumed that at least 1 phone per room is required. This means that 57% of houses will require 6 lines and 29% of house will require 8 lines. Using 8 lines gives enough lines to cover 86% of Australian households. It also allows more than one phone per room in the case of 6 rooms or less in a house.

Other Features

When each telephone in the house can be operated independently, many other possibilities that are not normally available open up. For example, the device can operate as an intercom, allowing inter-household calls. This is specially advantageous when a phone is needed in rooms or workshops detached from the main house.

Another potential feature is to route calls only to certain phones. For example, matching distinctive ringing patterns or caller ID, all business calls could be routed to the home office. After hours, they could be routed to an answering machine. Calls destined for one occupant of a household (such as a call for a teenage child at 2am) could be routed only to their rooms. The calls could also be re-routed, put on hold and other features normally only available at significant cost could be provided. The system also allows more than one phone call (incoming and outgoing) to occur simultaneously.

6.2 - Current Competition

When looking at this product, it is important to consider currently available technologies and how they compare with this device. The profitability of this device depends on its ability to be produced at a price point which is significantly below currently available solutions.

The device has a range of products which compete on number of lines OR price. However, no device available on the market currently matches a similar price per line as this project. Many of the other devices are stand alone and do not require a computer for basic functionality. However,

⁵ Australian Bureau of Statistics, (1999) "Australian Housing Survey -- Housing Characteristics, Costs and Conditions, 1999", http://www.abs.gov.au/AUSSTATS/abs@.nsf/ProductsbyTopic/53AF1D370FC826FECA256988007BF6A9?OpenD

http://www.abs.gov.au/AUSSTATS/abs@.nsf/ProductsbyTopic/53AF1D370FC826FECA256988007BF6A9?OpenD ocument

advanced setups (which are required for more than a couple lines) still required a computer. Some of the most prominent examples of competing devices currently on the market are compared below.

Linksys SPA2002-ER

Number of Lines: 2

Cost: \$US 59.95⁶

Inexpensive, easy to install and simple-to-use, the Linksys SPA2002 Analog Telephone Adapter connects a standard telephone or fax machine to IP-based data networks. IP telephony service providers and enterprises can offer residential and business users traditional and enhanced communication services via the customer's broadband connection to the Internet or Local Area Network (LAN).

The SPA2002 features two RJ11 POTS (Plain Old Telephone Service) ports for connection to existing analog phones, fax machines, PBX and key system communication platforms. The SPA2002 includes an RJ45 Ethernet port for connection to a home or office LAN. Each SPA service line can be independently configured via software controlled by the service provider and/or the end user.⁷

This is a comparable product produced by Linksys. This product does not require a computer to operate, however for more advanced functionality it would need to be used with one. But the device only supports 2 lines. To support the 8 lines this project required, it would cost \$US 239.80 and require a computer (to do the interdevice routing). This device is sold mainly by online VoIP providers as a simple solution for "entering the VoIP revolution".

BiPAC 6404V

Number of Lines: 2

Cost: \$US 165⁸

The world-standard Gateway feature known as "Least Cost Routing" enables users to choose the best VoIP call rates provided by various Internet Telephony Service Providers (ITSPs). Two integrated FXS ports provide dual lines for making VoIP calls. An additional FXO port enables you to make calls via PSTN Fixed-line while providing even faster Internet access sharing.⁹

This is a comparable product produced by Billion which targets the VoIP and home business markets. These devices are common because they also function as as ADSL router, with many

^{6 &}lt;u>http://www.bhphotovideo.com/bnh/controller/home?A=details&Q=&is=REG&O=productlist&sku=481367</u>

⁷ http://www.linksys.com/servlet/Satellite?c=L_Product_C2&childpagename=US%2FLayout&cid=1152745270028& pagename=Linksys%2FCommon%2FVisitorWrapper&lid=7002887006B02

^{8 &}lt;u>http://www.shopbot.com.au/p-26111.html</u>

^{9 &}lt;u>http://www.billion.com/product/voip/bipac6404vgp.php</u>

people ignoring the FXS ports. This product does not require a computer to operate in basic modes, but again, more advanced features require a computer. It would be unusual to try to support more lines with this device because of the high overhead cost.

Digium TDM880B

Number of Lines: 8 Lines

Cost: \$US 755.0010

The TDM800P provides an industry first with 8 standard two-wire, RJ-11 interfaces on a single PCI bracket. This eliminates the need for multiple brackets, external dongles, or splitters. In doing so, the TDM800P reduces part complexity, cable clutter, and points of failure.

Using this card in concert with Digium's Asterisk® software, standard PC hardware, and the Linux® OS, you can create SME or SOHO telephony environments capable of satisfying the needs of small or medium business applications at an industry-leading price.¹¹

The TDM880B is the most comparable to the device developed by this project. It requires a computer to operate and has 8 telephone lines. The TDM880B price point is significantly greater than this project as it is roughly 5 times the price the project is targeting. The TDM880B is quite popular in business set ups and would directly compete with the project's device in that market. The price point makes it prohibitive for the general home VoIP market.

¹⁰ http://www.digium.com/en/wheretobuy/digiumdirect/productview.php?product_code=1TDM880BF-01

¹¹ http://www.digium.com/en/wheretobuy/digiumdirect/productview.php?product_code=1TDM880BF-01

7 - Project Overview

The project went through a number of stages of development. Continual progress was made throughout the year. Some stages ran concurrently to make sure that the final goal could be reached.

The first stage was identification of the market and what the project would be required to do. So that the project could be successful, this stage was completed well before the project commenced.

The second stage was part identification and investigation. The aim of this stage was to investigate the feasibility of reaching the final outcome while remaining in side the identified requirements. This was completed before the first project proposal was submitted. The project proposal submitted outlined the scoping of the project and what would be done in the duration.

Once the project proposal had been submitted, the next stage was to source components and to test that their performance matched what was required. Each individual component was tested in various ways, such as on a bread board. The more vital parts were tested in more depth. Testing software was also developed where required.

Once each individual component was identified as working, integration testing started. During integration testing, several problems were identified which were not shown in the individual chip testing.

As the problems identified were not able to be resolved while the staying within the project constraints particularly remaining low cost the project underwent a system redesign and part replacement investigation. The replacement parts also underwent individual testing.

The next stage was to again try integrating the components. This time the integration was successful and a full prototype was created. Software which exercised the various parts of the system and tested the integration was also developed.

Using the skills learnt in the first prototype, a second prototype was created. The final demonstration software was also started. This prototype is the final product of the project and gives clear indication of how a final device could be produced at the price point desired.

8 - Project Changes

During development the device has undergone a number of changes. These refinements and modifications have been driven by trying to reduce the cost as much as possible, while still achieving the goal.

Conversion to CODECs

The most significant change from the original proposed design was the abandonment of the idea to replace CODEC with an external DAC and the PIC's inbuilt ADC.

The main reason this was abandoned was that the anti-alias filters required on each line were prohibitively expensive. The required filter would need to be an 8th order elliptical filter. While this can be implemented using passive components, it would require a minimum of 8 capacitors and 8 resistors. While the cost of each of capacitor is only a few cents, the system needs 8 of these (one for each line) causing a significant cost increase.

If the filter route had been pursued, the production cost of the device would have rapidly blow out as the cost of the DAC and filters were significantly more than the cost of two quad CODEC devices.

The second reason for abandoning using the PIC's in built ADC was that the required sample rate needed for 8 lines, while theoretically possible, was not practically possible. This could have been solved by reducing the number of lines in the device – but this would have resulted in an increase in the price per line.

Instead it was decided to replace the DAC and filters with two quad line CODECs. The National TP3094 PCM CODEC was chosen because of the ease of getting samples and the low cost of purchase in small quantities (~100 units). It is likely that production revisions of this device would instead using a more advanced CODEC. A variety of these CODECs can be found for a similar price point when purchased in larger numbers (~10k units). However, sourcing samples of these more advanced devices turned out to be significantly harder than for TP3094, so the prototype did not go down this route.

The TP3094 chip also required that the line balancing be done by external passive components. However, with cheap telephones and on poor quality lines, voice quality is degraded, nor does it allow advanced functionality such as volume control. In the final device the more

advanced CODECs using a digital filter on the input would be used, allowing for much greater control.

One problem with converting to using CODECs was that the PIC does not contain a PCM interface. An external PCM interface chip could have been used to facilitate this situation, but again this would have driven costs up. Instead, the SPI interface was repurposed to be used as a PCM interface. This produced a number of problems that had to be resolved in software, but kept the cost down.

The PIC also had no way to generate the clock needed by the PCM highway. This required adding an oscillator to produce this clock signal. While oscillators of the right speed are quite expensive when purchased in small amounts, when purchased in batches of 1k lots, the price drops significantly.

Removal of Port Extender

The port extender was adding significant cost to the device for limited extra functionality. After further analysis, much of the functionality of the SLIC chip was not required, including:

- Ground Key Detect
- All modes using pin F0.

By tieing these IO pins to specific levels, the number of IO pins required was reduced. It also meant that serial shift registers could be used instead of the Port Extender.

The shift registers chosen are the 74HC595 – Serial to Parallel Shift Register with Output Latch, which is a standard chip in the 74HCxxx range. This means that the IC can be easily sourced from many different manufacturers, which gives the customer significant leverage when negotiating price. As well, the same IC was used for all the shift registers.

It is estimated that this reduced the cost by \$US3.33 (from \$US4.37 to \$US0.66), but because of the significant leverage in negotiating the price of these registers, the savings could be more significant in commercial production.

These registers could even be removed by using the new higher IO PIC. This is only feasible because of the reduced number of IO needed. This is discussed in more detail in the "Further Development" section.

Block Diagram

The original block diagram for the system is shown in Illustration 1. After incorporating the CODEC and shift registers changes, the block diagram now appears as seen in Illustration 2. It can be seen there is still considerable similarity between the diagrams.



Illustration 1: Original System Block Diagram



Illustration 2: Final System Block Diagram

9 - Project Progress

USB PIC – Breadboard Prototype

The first step in the project was to prove that it was possible to communicate with the PIC 18F4455 device via USB. To do this, the PDIP version of the chip was used in a breadboard and the code examples from Microchip were downloaded to the device. The resulting breadboard circuit is shown in Illustration 3.



Illustration 3: USB PIC – Breadboard Prototype Picture

The chip worked as described, but the limits of the breadboard were quickly reached.

USB PIC – Veroboard Prototype 1

As the limit of breadboard had been reached, the project moved to using a veroboard prototype, as seen in Illustration 4. This prototype was used to test various features of the PIC, including how to produce reliable outputs and inputs. How to produce outputs on the SPI interface was also researched and tested.



Illustration 4: USB PIC – Veroboard Prototype 1 Picture

This prototype did not include any USB interface.

USB PIC – Veroboard Prototype 2

With the lessons learned from the first veroboard prototype board, a second prototype was created. This new board included a USB interface and a connector for interfacing the external SPI peripherals. This board was very useful in debugging various problems when communicating with the DAC and Port Extender devices. A picture of this prototype can be seen in Illustration 5. This device was functional that is was used by the "GSM Payphone (MJS1/2)" to kick start their initial development.



Illustration 5: USB PIC – Veroboard Prototype 2 Picture

USB PIC – Milled Prototype

As the final device would need to be put onto a PCB board, two PCB prototypes were designed. As the project was using the CadSoft Eagle PCB software, rather than Altium, these prototypes made sure that the process for producing PCBs was understood. As well, these boards gave an understanding of what was needed to produce a working PCB based around the PIC microprocessor. Illustration 6 shows the first low density design, while Illustration 7 shows the higher density design.



Illustration 6: USB PIC – Milled Prototype (Large Version) Picture



Illustration 7: USB PIC – Milled Prototype (Small Version) Picture

SLIC Chip – Breadboard Prototype

One of the most important parts of the device to get working was the Subscriber Line

Interface Chip (SLIC). This would be used for interfacing to the telephone line. To get the SLIC to work a converter was created which allowed the PLCC chip to be put on a breadboard. This board was also used to work out what the minimum ringing signal requirements were for most phones. The digital signals were simulated by using DIP switches and LEDs, while the analog signals were created using signal generators and observed on a CRO. Illustration 8 shows this breadboard prototype.



Illustration 8: SLIC Chip – Breadboard Prototype Picture

Care was taken to make ensure that the -48V DC power supply was not routed through the breadboard.

SLIC Chip – PCB Prototype

After a circuit design had been created the next stage was to create a PCB design. As this design would be used as daughter boards on the final device and 8 were required, care was taken to make it as small as possible. SMD components were used to help reduce size. The board was milled at the University to ensure that it was correct. The milled result is shown in Illustration 9.



Illustration 9: SLIC Chip – Milled Prototype Picture

Once the design was tested, the PCB was commercially produced. Illustration 10 shows the result. As these commercial produced PCBs had a solder mask, they were more reliable than the milled prototype. These completed boards are referred to as Telephone Interface Modules (TIM).



Illustration 10: SLIC Chip – TIM Module Picture

As these boards provided a complete design interface for interfacing to a telephone, the "Design an 8-Port Stand Alone Telephone Exchange (MS1/2)" project decided to purchase four modules to help reduce their development time.

Port Extender Chip – Breadboard Prototype

The port extender was originally planned to be used to extend the number of IO ports. This was tested by prototyping on a breadboard. As the port extender can not be used on its own, it was

interfaced with the Veroboard Prototype 2 board via a ribbon cable. This also tested the SPI communication of the Veroboard Prototype. Red LED bars were used for testing output, while a block of DIP switches was used for input, Illustration 11 shows this set up.



Illustration 11: PE IC – Breadboard Prototype Picture

A video of this output can also be found in the code repository. This shows the lights been consecutively light up and the input from the switches are copied to the bar LEDs on the prototype board.

DAC Chip – Breadboard Prototype

The DAC chip was also tested in a similar manner to the port extender. With this testing the chip was interfaced to the USB PIC – Milled Prototype instead of the Veroboard version. The output was measured on a multi-trace oscilloscope. The prototype was inadvertently dismantled before photographs could be taken of the device.

CODEC – Breadboard Prototype

Once the change to using CODECs had been decided on, the CODEC also needed to be prototyped on a breadboard. As the CODEC had tight timing requirements, it was vital to prove that the PIC was able to generated the required signals.



Illustration 12: CODEC IC – Breadboard Prototype Picture

During this prototype phase, it was discovered that the PIC board was not able to produce the required master clock, hence the design was changed to incorporate the external oscillator.

Prototype Board – Milled Prototype 1

As all the parts had been proven to work individually, the next step was to test an integrated system. The first full system design was milled by the University and is shown in Illustration 13.



Illustration 13: System Board – Milled Prototype 1 Picture

A number of problems resulted from not taking into account the manufacture process of the

board, and the board was not fully functional. The close tracks and small pads meant that numerous shorts occurred during testing. After some success, a short which occurred under one of the CODEC chips required one CODEC to be removed. Illustration 14 shows the result after the professional had technicians removed the chip.



Illustration 14: Chip Removal Damage

As can be seen this left the pad totally unusable. Luckily the other CODEC was not effected and more testing was still able to occur.

Another problem encountered was the lack of easily accessible test point, requiring wires to be soldered into vias.

The board was used to developed software to test various functionality and a number of features were proven to work using this board, these include:

- writing to the shift registers (which had not been previously tested)
- writing samples to the CODEC chips.

Because of the numerous shorts, applying a -48V supply required by the TIM modules was too risky so the TIM module functionality could not be tested.

Prototype Board – Milled Prototype 2

After consideration of the previous prototype, the design was adapted to be more compatible with the process. The opportunity was used to also switch to SMD shift registers and add numerous

test points. This design was again milled on the University board and shown in Illustration 15. As consideration had been given to the production process - shorts, while still occasionally occurring, were not a significant problem.



Illustration 15: System Board – Milled Prototype 2 Picture

This board was the first to produce a tone from the PIC all the way to the telephone. On this board it was proven that the PIC was able to change the TIM modes and get a telephone to ring.

Prototype Board – Commercial PCB Prototype

To make sure that the final prototype device was not as fragile as a board produced via the milling process, the same design was also sent to Entech to be produced on their commercial PCB process which includes a full solder mask and silk screen. One of the resulting PCB boards is shown in Illustration 16. A populated board is shown in Illustration 17.



Illustration 16: System Board – Commercial PCB Prototype Picture



Illustration 17: Populated Commercial PCB Board

Development on this board was significantly easier a previous milled prototypes and all work was switched to these boards when they became available. The final demonstration software was able to be produced much more quickly on this board.



For comparison between the boards they have been shown side by side in Illustration 18.

Illustration 18: Prototype Boards Compared

10 - Risk Management

Risk management played a key part in making this project successful. The project has been challenged by a large number of potentially damaging problems. However proper planning has mitigated most of the risks and the impact on the final outcome has been kept to a minimum. The fact that there was a significant change late in the project design is the main reason why the ultimate goal of actually producing a board ready for commercial production was not reached.

Some of these risks, how they were managed, and the impact on the project have been examined. Suggestions for improving the management of these risks are also discussed.

10.1 - Computer Related Risks

The project had two major computer related risks occur over the duration of the project. These type of problems have had significant impact on other projects in the past, hence the risk mitigation was well understood and enacted.

The first risk was a very common one facing computer users; that of failure of the hard drive in the critical phase of a project. To mitigate this risk, a revision control system was used. This allowed the code resources to be stored and easily replicated on a number of computers. At any one time the code in various states existed on 4 independent computers (not including the server code repository).

The second risk was the potential for a malicious user to modify or destroy data stored on the computer (including the code repository). In fact, the server was compromised and the hacker was able to get administrator privileges, which meant that they could have potentially modified the code to include malicious programs. This risk had been mitigated by the fact that the backup was a RCS server rather than a simple flat file backup. This meant that the hacker was unable to change any code without corrupting the repository and the code was easily checked against the checked out repositories on the other computers.

10.2 - Design Based Risks

Filter Expense

As previously discussed, the board was not able to use filters for cost reasons. This problem

was compounded by the fact that the PIC ADC claimed a sample rate of 160kSps, however this was not practically possible.

As a development project, an extended timeline had been built into the project's timeline to mitigate problems encountered such as this. This discovery, however, occurred late in the project, so while the impact was significantly reduced by proper management, there was still an impact on the actual final outcomes of the project.

CODEC Behaviour

Another problem that occurred was that the CODEC behaviour was significantly different to what had been expected when designing the original board. This meant the software was significantly more complicated than originally planned and took longer to develop. This problem was discovered early on and to mitigate this risk, the scope of the final software was reduced which allowed it's completion.

Power Supply

Power supplies in any circuit have a potential to do damage to devices. While the significance of this risk and potential impact on the project was considered, the choice of not having power protection circuitry was made to keep the cost down. Instead of protection circuitry the board was dependent on a polarised connector to prevent reverse polarity. This did not take into account that the polarised connectors needed to be connected to the supply during the prototype phase and no safeguards against accidentally switching the lines was provided.

A small mistake two weeks prior to the project deadline were the wrong polarity was connected resulted in massive damage to the original prototype system and all devices on the board were completely destroyed.

While the significance of this should have been more carefully considered, another board was able to be produced quickly as all ICs had originally been procured in amounts which allowed production of up two 3 complete boards. This enabled the project to continue to the stage shown in this document.

Software Problems

After the first board was damage, the software did not perform on the new board although it

had on the first board. This problem was tracked down using the RCS to examine previous developments and tests. Without the RCS, the fault would probably have been impossible to find, requiring software development to start from scratch. This highlights the importance of including such mechanisms in development projects.

10.3 - Supply Chain Risks

PCB Manufacture

An important part of the development was the production of PCBs. The University's milled boards were chosen because of the speed of the turnaround. However, the University boards where very hard to work with when using the ICs that were chosen. This had not been anticipated and meant the boards required more than one revision. Numerous shorts occurred slowing development on the board.

The board needed to be redesigned to reduce the possibility of these shorts. The production of this new board, however, was delayed because the staff member with the skills to the manufacture the PCB retired from his position at the university with no immediate replacement. To work around this problem, the board was also sent for commercial production. This turned out to be highly advantageous as it removed all the shorting problems.

11 - Project Spending

The following tables show how the project budget was spend during the development process.

Date	Component	Qty	Price	Total
29/11/06	CAPACITOR, 1206 4.7UF 10V	30	\$0.38	\$11.43
12/07/2006	LED, SMD 0603 R/A RED	25	\$0.29	\$7.25
12/07/2006	LED, SMD 0603 R/A ORANGE	25	\$0.29	\$7.25
12/07/2006	LED, SMD 0603 R/A GREEN	25	\$0.29	\$7.25
1/09/2007	TIM PCB Manufacture	1	\$200.00	\$200.00
12/02/2007	4.096MHz Crystal Oscillator	2	\$10.20	\$20.40
2/03/2007	74HC595 - 8 bit shift register with output latch	5	\$0.85	\$4.25
	Sold Tim modules to Chun Khai Gan	4	-\$35.00	-\$140.00
4/12/2007	ZVC 2pin univ input SMPS adaptor 48V 65W	1	\$92.57	\$92.57

Table 1: Project Spending

Some items where also procured at no cost through other means. They are listed below:

University of Adelaide

Commercial PCB Production of Prototype

Miscellaneous Components from Store Stock

Milled Prototype Boards

Usage of Bench-top Equipment

MITHIS

Surface Mount Resistors and Capacitors

Surface Mount LEDs

Surface Mount 74HC595 chips

Microchip Samples Program

8 x PIC18F4455 - Microchip 18F Series PIC with inbuilt USB

8 x PIC18F4550 - Microchip 18F Series PIC with inbuilt USB

Intersil Samples Program

25x HC55185 – Ringing SLIC for Short Loop applications

Texas Instruments Samples Program

4 x DAC Samples – 12bit, 8 Channel DAC

National Samples Program

10x TP3094 – Quad PCM CODEC/Filer

Maxim Samples Program

2 x MAX7301 – 28 IO Port Extender

12 - Production Budget

The following tables (Table 2 and Table 3) outlines the predicted cost to mass produce the **prototype device** in batches of 1000 or greater. This clearly shows that even in the current form the device should be able to be produced at under \$US 100.

While at this cost the target of retailing for \$US 150 can not be matched, these costs are for the prototype device which is significantly more expensive. With further developments the cost of production device could easily be reduced below the \$US 50 mark. This would allow the device to be marketed at around \$US 150 point making it extremely competitive.

The tables includes all the costs for purchase and manufacture of all parts (including PCB) and the complete construction. Where estimated costs are uncertain extra margins have been added.

		Numbers b	based on producing items in 1k lots				
		Cost reduction	on by replacing 18F4455 with more IO		C	ost Per Port	\$12.40
	Cost reduc	ction by replace	cing TP3094 and HC55185 with combined device				
		Cost highly	dependent on board size/part count				
Supplier	Part Number	Package	Part Description	No	PPI (\$US)	PPI (\$AUS)	Total Cost (\$US)
Microchip	PIC18F4455-I/PT	TQFP 44	PIC18F4455	1	\$4.75		\$4.75
ΤI	SN74HC595D	SOIC 16	74HC595 – Shift Registers	4	\$0.33		\$1.32
National	TP3094	PLCC 32	TP3096 – CODEC	2	\$5.05		\$10.10
		603	Resistors – Various	45		\$0.02	\$0.90
		805	Capacitors – Various	13		\$0.10	\$1.00
		SOD83	Diode – Various	3		\$0.40	\$0.92
		603	LED – Various	3		\$0.25	\$0.58
		DIP 14	4.096MHz Oscillator	1		\$4.00	\$3.08
		603	LED	3		\$0.20	\$0.46
		HC18U	4MHz Crystal	1		\$1.00	\$0.77
			TIM Modules	8	\$6.37		\$50.96
		PN61729	USB Connector	1		\$1.00	\$0.77
			Power Connector	1		\$1.00	\$0.77
			48V Plug Pack Power Supply	1	\$8.00		\$8.00
			PCB Board Manufacture PCB Board Assembly	1	\$11.00		\$11.00
			Case	1	\$4.00		\$4.00

\$99.38

Total

 Table 2: Prototype Board Production Costs

Part Number		Part Description	Reference	No	PPI (\$US)	Total Cost (\$US)
					Total	\$6.37
	PIN Header			1		\$0.00
	RJ12 Connector			1	\$0.25	\$0.25
HC55185ECR	SLIC, Ringing, VoIP,	75/85/100V, Gnd Start, LB = 53/58dB		1	\$4.48	\$4.48
	1206 Capacitor	4.7uF	CDC, CFB	2	\$0.18	\$0.36
	0805 Capacitor	0.1uF (Decoupling) – 50V	CPC, CPSH	2	\$0.10	\$0.20
		470nF (Filtering)	CRT, CRX, CTX	3	\$0.18	\$0.54
	0603 Resistor	47 (50 preferred)	RPR, RPT	2	\$0.02	\$0.04
		18k	RTL	2	\$0.02	\$0.04
		22k	RRT	1	\$0.02	\$0.02
		47k	RSH	1	\$0.02	\$0.02
		68k	RIL, RS	1	\$0.02	\$0.02
	SOT80 Diode		DALM	1	\$0.40	\$0.40

 Table 3: TIM Module Production Costs

13 - Commercial Device

There are a number of differences between the prototype board and the potential final commercial device. The prototype board includes a number of features to speed development which make little sense when in commercial production. Other details, such as packaging and marketing, not considered in the prototype; are important once the device is being produced.

13.1 - Size Reduction

The prototype board is significantly bigger then the final product would be. A reduction in size would be achieved by:

- integrating the TIM daughter boards as part of the main board,
- moving to smaller packages,
- moving to 4 layer board.

It is estimated that this would to reduce the size by 40%. This would be in line with many other products currently on the market, such as network switches and wireless routers.

13.2 - Packaging

For an example of what the final device might look like, network switches were examined. These devices share very similar external requirements, for example they have a large number of RJ sockets and only do limited processing. Illustration 19 shows some examples of packaging of some currently available network switches. The image on the left is a metal case, while the image on the right is a plastic case.



Illustration 19: Possible Packaging Examples

As the device is fundamentally different to these products, it is clear that the packaging of the device needs to be different enough so that it is not confused with these other types of products.

This type of packaging is also suitable for the Ethernet system discussed in the "Further Developments" section, meaning that the moulds could be shared between these systems – reducing the cost of packaging significantly.

Another possibility is for the device to be designed so that it can be placed internally in the computer. The device would be well suited to be mounted in the 5-1/2 inch drive bays found in a computer. This would remove the need for external casing, further reducing cost. This would however not be suitable for the Ethernet device, which has the advantage of being able to placed away from the computer.

13.3 - Using Different CODEC

As discussed in the Project Changes section, the current CODEC chip being used (the National TP3094) is not the most suitable for the final commercial device. Instead a digital CODEC should be used. A number of options have been examined. All these chips have the advantage that the hybrid balance can be dynamically changed, allowing features like volume control to be added.

IDT 82V1054A

This chip is produced by IDT and specifically designed to work the the HC55185 SLIC chip used in the TIM modules. The chip uses a serial interface for communicating with the CODEC, with would reduce the number of IO ports needed. The chip also includes IO lines to be connected to the SLIC chips which removes the need for the shift registers which are connected to the TIM modules.

SI Integrated CODEC

SI Labs produce a number of "integrated" chips. These chips integrate both the features of the CODEC and SLIC chips allowing the TIM modules to be totally removed. As there are 8 TIM modules, this could drastically reduce the cost of the device.

Legerity Integrated CODEC

Legerity also produce "integrated" chips. These chips would have the same advantage as the SI Integrated CODECs. Unlike other companies, these chips are designed to be used in VoIP devices rather than standard telecommunications equipment. This means that they offer features such as wideband operation and high fidelity capture rate. Pricing on these chips is not public

available so the potential impact on the overall cost is not known.

14 - Further Developments

There are a number of developments which could still be done for this project. They are divided into two main categories, "Cost Reduction" and "Feature Enhancement". These categories are not mutually exclusive as some feature enhancements can also introduce a cost reduction and these have been noted where they are likely to occur.

Cost Reduction Developments

Combining of Shift Register data lines

This is a very simple change and will probably be added to the next prototype boards. As data is only shifted in when the clock line changes, the data lines could be multiplex together. This would reduce the number of pins required by 3, freeing them for doing other operations, such as sensing connection of the 48V power supply.

High IO USB PIC Version

The current system relies on a PIC 18F4455, this PIC has limited IO so serial shift registers have to be used to add enough IO to talk to all devices. In recent weeks a high IO version of these PICs has become available (PIC18F8xJ50). This new IC would allow the shift registers to be removed. This would decreases the overall costs for a number of reasons:

- Reduction in part account (both individual and total number)
 - Smaller cost of inventory
 - Smaller cost of production
 - Better economy of scale
- Higher density printed circuit board
- Reduction in software complexity
- Reduction in failure modes.

Replace PIC with DSP processor

The PIC processor was chosen for the ease of programmability and large number of free tools.

The PIC however, only has enough power to move bits around the various sub-systems. By replacing it with a DSP – which can be purchased for approximately the same cost, the device would be able to do a large amount of processing on board (such as echo cancellation and DTMF detection) and it might even remove the requirement for connecting to a computer.

Higher Density Chip Version and Small SMD components

Both the PIC chip and SLIC chips come in higher density versions. As well, all 0603 resistors could be replaced with 0402 resistors. By replacing the chips with the higher density versions, the PCB board could be significantly smaller, which would reduce the cost of PCB production. The chips are also lower in profile, allowing for a smaller overall package.

Illustration 20 shows the size difference between the high density QFN and lower density PLCC versions of the Intersil HC55815 chips used in the TIM modules.



Illustration 20: Intersil HC55185 - High Density QFN compared to PLCC

Feature Enhancement Developments

Ethernet PIC Version

The system is based around a 18F4455 PIC which has an inbuilt USB Interface. An almost identical device, the 18F60J90 also exists with inbuilt Ethernet interface instead of a USB interface.

Only a small amount of code and hardware design would have to be changed to use the Ethernet device and none of these changes would affect the "hard part", that is the telephony side. This would be a significant feature as it would allow placement of the device a long way from the

PC (up to 100m without any extra devices and almost unlimited with intermittent switches) and allow a significant number of the devices to be used together.

The cost of using the Ethernet device would be of only small significance (in the order of \$US10). As the device could use Power over Ethernet, this could be easily offset by not having to supply a "power brick" that is needed by the USB version.

As well, the economies of scale because of the 90% common parts between the Ethernet and USB versions would mean that it would reduce the cost of both devices.

Asterisk PBX Interface

Asterisk PBX is the most popular software based PBX available. By creating an interface between this device and Asterisk a large number of features become possible. Asterisk supports all major VoIP protocols and would allow communication between devices using these protocols and the device. This further development is very important to the final commercial success of the project and will definitely be attempted.

Line Line Support

Another possible support is adding "life line"¹² support. This feature however has a number of drawbacks as once the device is connected to the standard PSTN network it requires certification by the ACIN authority. This certification is expensive and requires that the device perform to very stringent standards.

Direct Connection

The demonstration software has shown that the device could theoretically work independently from a PIC. This feature could be further developed so the device could be sold as stand alone, not requiring a computer. For more advanced functionality this would require a significant investment in software development. Some aspects, such as doing things similar to DTMF decoding (of multiple lines simultaneously), would be a significant challenge.

¹² Lifeline support is where the device will turn into a piece of wire and directly connect the telephone to the PSTN network when the device has not power.

Appendix I - Technical Document – MITHIS CFXS Datasheet

This page intentionally left blank

Appendix II - Further Background Information

14.1 - Internal Telephone Interface Cards

Internal Telephone Interface cards are devices which are put inside the computer and communicate directly over internal buses. These are generally PCI cards, such as the TDM400P produced by Digium¹³. These devices generally do a large amount of processing internally. This can include DTMF detection and generation, echo cancellations and other such functions.

When computers were not powerful enough to do the processing in software, this internal processing was specifically required. However, today this is not a concern as processing power is both cheap and easily upgraded. Software systems these days can also often produce better results for these processes, meaning that this internal functionality is often not used.

VoIP Handsets

VoIP Handsets come in two forms. The first type plugs directly into the network. These devices generally must talk to a gateway server, but this can often be at a remote location. They are also generally only able to understand one protocol, meaning they are unable to talk to many users.

The second type plugs into the computer by an external bus, such as USB. One example is the Cyberphone K USB Skype Handset¹⁴. These devices are generally nothing more then a sound card and keypad, leaving the computer to do any processing. The major problem with these devices is that they must be directly connected to a computer and cannot be used from various locations within a premises.

Gateways

Gateways are devices which do the complete processing internally and require no connection to a computer. They normally connect directly to a network and are able to work completely independently from a computer. These devices are often limited in their ability to route calls, so they are often still used in conjunction with computers to achieve the more advanced functionality.

These systems are also often tied to only one protocol, such as SIP or H323. There are no known gateway systems which interface with Skype. This limits the number of people who can be

¹³ Digium, "TDM400P", http://www.digium.com/en/products/hardware/tdm400p.php

¹⁴ Firebox, "Cyberphone K USB Skype Handset", http://www.urban75.org/tech/skype_cyberphone.html

called using this technology.

Appendix III - List of Acronyms

ACIF	Australian Communications Industry Forum
ADC	Analogue to Digital Converter
DAC	Digital to Analogue Converter
FXS	Foreign Exchange Station
IETF	Internet Engineering Task Force
IEEE	Institute of Electrical and Electronics Engineers
ΙΟ	Digital Input or Output line
IT-U	International Telecommunication Union
PBX	Private Branch eXchange
PE	Port Extender
PSTN	Public Switch Telephone Network
SIP	Session Initiation Protocol
SPI	Serial Peripheral Interface
TIC	Telephone Interface Chip
TIM	Telephone Interface Module
USB	Universal Serial Bus
VoIP	Voice Over Internet Protocol